PTO-1449 REPRODUCED

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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(Use several sheets if necessary)

ATTORNEY DOCKET NO.	APPLICATION NO.
2789.2001-001	09/557,640
APPLICANT: William J. Dally et al.	
FILING DATE: 04/25/00	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	TRANSLATION NO
	AL							
	AM							
	AN							

OTHER DOCUMENTS ***(Including Author, Title, Date, Pertinent Pages, Etc.)***

JT	AR	Dally, William J. and Poulton, John W., *Digital Systems Engineering*, Cambridge University Press, 1998, pp. 428-447, 537-540 and 547-548.
JT	AS	Kim, Weigant and Gray, "PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design," ISCAS, 1994, pp. 31-34.
JT	AT	Waizman, A., "A Delay Line Loop for Frequency Synthesis of De-Skewed Clock," IEEE International Solid-State Circuits Conference, 1994, pp. 298-299.
JT	AU	Dally, William J. and Poulton, John W., "Transmitter Equalization for 4Gb/s Signaling," IEEE Micro, Jan-Feb 1997, pp. 48-56.

EXAMINER	DATE CONSIDERED
Thuan	09/01/03